Complementary JFET Offset Mismatch

The full complementary JFET input stage of the DH-220C comprises two pairs of dual monolithic JFETs, one a P-channel pair and the other an N-channel pair. Each pair is loaded with a current mirror that tries to make the current of both devices in a given pair equal. However, each pair may have voltage offset of up to ±20 mV. If the offsets of the N-channel (Q9A & Q9B) and P-channel (Q10A & Q10B) pair are the same and in the same direction, the only consequence will be a slight DC offset at the output of the amplifier (which will actually be corrected by the DC servo).

If, however, as in the real world, the offsets of each pair are not the same, it will not generally be possible for the drain currents to be the same, since the gates of the two pairs are connected together. Thus, the two pairs will fight each other for control of the offset. This will cause the VAS bias current to be different from its design value, either higher or lower. Figure 1 is a simplified schematic of the input circuit to help illustrate this effect.

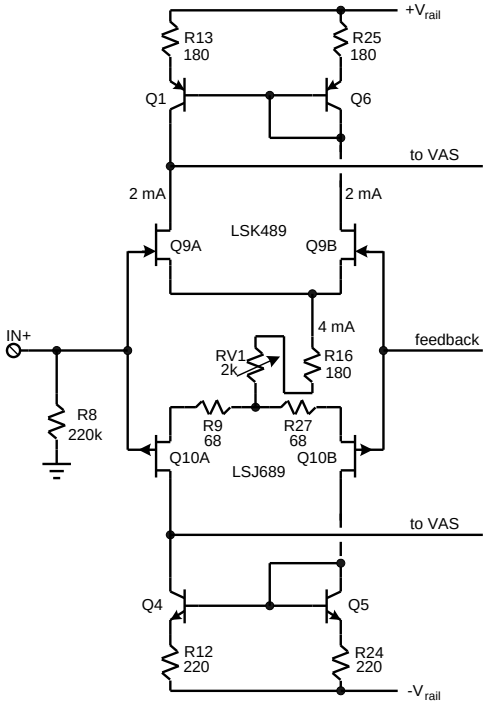

Figure 1: Simplified Schematic of the DH-220C Input Stage

Tolerance to VAS Bias Current Differences

This design is very tolerant of VAS bias current over a wide range and performance is not strongly affected by it. The amplifier can actually operate quite well over a range of 5 mA to 20 mA for the VAS bias current. The design value of 10 mA is actually a bit arbitrary. With too small a VAS bias current, maximum slew rate will begin to be affected. With too high a VAS bias current, dissipation in the VAS transistors will

cause them to operate at a higher temperature than desirable. In this design, it is desirable for the VAS bias current to be between 7.5 mA and 15 mA.

Definition of JFET Offset Difference

As mentioned above, what matters in this regard is how much *difference* in offset there is between the N-channel pair and the P-channel pair. JFET pair offset here is defined by the value of V_{gs} of device A minus the value of V_{gs} for device B in each pair. Thus, if the N-channel pair has offset of +10 mV and the P-channel pair has offset of +10 mV, and they are both fed an offset voltage of 10 mV, both pairs will have their drain currents of device A and device B be the same. Here the difference in offset voltages is zero. Under these conditions, the circuit is balanced and the two pairs do not fight each other.

An undesirable case would occur if the N-channel pair has an offset of +10 mV and the P-channel pair has an offset of –10 mV. Now the difference in offset voltages is +20 mV, and the two pairs will fight each other, causing the VAS bias current to be altered from its design value. Figure 2 illustrates JFET pair offset differences and shows how to measure it. In the figure, the JFETs are operated at approximately 2 mA, just as they are in the DH-220C input stage. This figure also shows how the offsets and differences in offsets are defined.

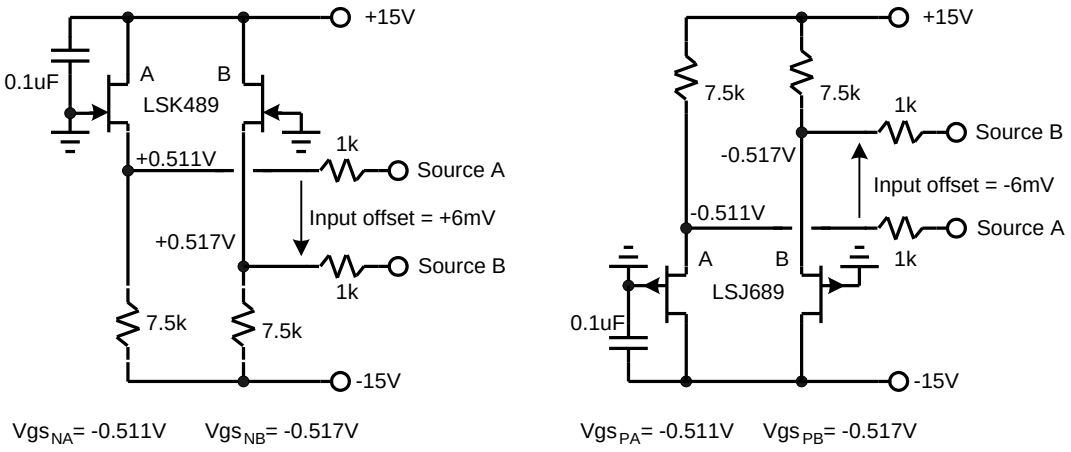

Figure 2: Measuring JFET Pair Offset Voltages

VAS Bias Current Sensitivity to JFET Pair Offset Difference

Some example numbers show how VAS bias current changes with amount and polarity of offset between the two pairs.

SPICE simulations indicate that a +10 mV JFET offset difference will decrease VAS bias current by 1.0 mA. In other words, if Q9A required +10 mV on its gate compared to all 3 other JFETs that were equal in order for Q9A to conduct the same current as the others, corresponding to a +10 mV JFET offset difference, then VAS bias current would be 1 mA less than its nominal value. Conversely, a –10 mV JFET offset difference will increase VAS bias current by 0.9 mA.

JFET Installation Reversal to Reduce Offset Effect

The packaging of the TO-71, 6-lead device, if installed in an IC socket, allows the insertion of the device to be flipped around easily, with the only result being the interchange of the roles of device A and device B. This will reverse the polarity of the offset of the device. In the undesirable case where the offsets of the two dual devices is opposite, with the N-channel offset being +10 mV and the P-channel offset being –10 mV, if the P-channel device is flipped, its offset as seen by the circuit will become +10 mV. In this case, the offsets of the P-channel and N-channel devices will be the same and the circuit will be balanced. Of course, the magnitude of the offsets of the two pairs will usually be different. If the N-channel device has offset of +10 mV and the P-channel device has offset of –6 mV, the net difference in offset is 16 mV. If the P-channel device is flipped, the net offset then becomes +4 mV. The bottom line is that one device can usually be flipped to achieve substantially lower net offset. If devices cannot be flipped, there are other ways to trim the circuit and bring the VAS bias current to within the desired range of 7.5 mA to 15 mA.

Trimming P-channel Source Resistors

One approach is to tweak the values of the P-channel source degeneration resistors R9 and R27 to be different. This creates an effective voltage offset in the P-channel portion of the arrangement without changing operation very much, since the floating tail resistance is significantly larger than that of these resistors. These resistors normally serve to decrease the transconductance of the P-channel pair to match that of the N-channel pair. With 2 mA flowing in each transistor, the voltage drop across each 68-Ω source resistor is 136 mV. It is easy to see that making a modest difference in the value of either of the two resistors can provide enough synthetic offset to cure the offset issue. The value of device Q10A's source resistor required to counter the offset as a function of the initial VAS bias current observed can be determined by measuring the VAS current and knowing what the sensitivity to source resistor value is. The sum of the source resistors for device Q10A and device Q10B need not remain at exactly 136 Ω, so it is OK to make the trim by just shunting one or the other of the source resistors. The actual value of the tweaked source resistors is obviously not critical.

SPICE simulations indicate that decreasing Q10A's source resistor R9 by 10 Ω to 58 Ω, VAS bias current will be increased by 1.9 mA. Decreasing Q10B's source resistor R27 by 10 Ω to 58 Ω decreases VAS bias current by 1.8 mA. Decreases in source resistor values are described because they can easily be implemented by soldering an additional shunting resistor to one of the source resistors. The minor change in total source degeneration of the P-channel pair as a result of such trimming has only a small effect on amplifier performance.

Adjustment of IPS Tail Current

The VAS bias current in the DH-220C increases and decreases with increases and decreases in the IPS tail current. Although the nominal IPS tail current is recommended to be set to 4.0 mA during the amplifier adjustment procedure, the truth of the matter is that the 4.0-mA number is a bit arbitrary, and amplifier performance is quite tolerant of minor changes in this current as long as the VAS bias current ends up within its fairly broad recommended range. This means that if the JFETs cause the VAS bias current to land a bit outside of its range, adjustment of the IPS bias current in the range of 3.5 mA to 4.5 mA is another approach available to achieving the desired VAS bias current.

I_{DSS} and Threshold Voltage Matching

Some may ask if the N-channel and P-channel JFET pairs need to be matched for I_{DSS} and/or threshold voltage when used together to form a full-complementary differential input stage, as implemented in the DH-220C. The answer for this design is no. It is just the sum of the gate depletion voltages at 4 mA per pair that determines the IPS bias current, and that is adjusted by VR1. The gate voltages naturally find their own value. For the same reason, I_{DSS} of the P-channel pair does not need to be matched to the I_{DSS} of the N-channel pair. There is an interesting property of JFETs that reduces the importance of matching I_{DSS} in certain circuit applications. That has to do with the desire to have the operating transconductance of the N-channel differential pair be about the same as that of the P-channel differential pair when operating at the same current, which they do in this design.

Neither I_{DSS} nor threshold voltage, by themselves, determine the operating transconductance of a JFET. For JFETs, transconductance is mainly set by the parameter Beta, which is one of the parameters in the JFET SPICE model (not to be confused with BJT current gain). Unlike I_{DSS} and V_t, Beta is pretty much the same from batch to batch of JFETs made in the same process. Operating 2 JFETs at the same current will yield transconductance that is in the same ballpark even if those JFETs have differing I_{DSS} or V_t. Even though I_{DSS} and V_t can vary quite a bit for JFETs, it turns out that Beta is much better controlled and lies within a smaller range [1].

This property of JFETs made it practical to parallel 4 pairs of un-matched LSK389 JFETs in the VinylTrak moving coil preamp to achieve extremely low noise while still using a differential input topology [2]. The key to making this work was to provide each of the 4 pairs with its own tail current source.

That having been said, the transconductance of the P-channel LSJ689 is a bit higher than that of the N-channel LSK489 when they are both operated at the same current. That is why the sources of the LSJ689 differential pair are degenerated by R9 and R27 – it nominally equalizes the net transconductance of the pairs.

Procedure

Reversing one of the devices will often adequately address the issue, but that is only practical for the devices in TO-71 cans, that are installed in a socket.

If you are using the SOT-23 devices, the best approach is to tweak one of the LSJ689 source resistors by putting a resistor in parallel with it. Such a resistor might cause the value of the associated source resistor to decrease by 10% or 20%, for example. The procedure is straightforward. The idea is to build the board as per the schematic and then, if needed, attach a parallel resistor on the component side of the board across one of the 68-Ω source resistors as needed. A 10% reduction in resistance of one of the resistors will correct a significant amount of offset difference between the two pairs. This is easy to understand by recognizing that each 68-Ω resistor has about 2 mA flowing through it, creating a voltage drop on the order of 135 mV. Reducing one of those resistors by just 10% provides an offset compensation of about 13 mV. A 750-Ω parallel resistor will reduce the resistance of a 68-Ω resistor by about 10%.

Adjust the IPS tail current to 4 mA, using RV1. This can be done by either measuring the voltage across the fixed resistor between the sources (R16) or by

monitoring the voltage across one of the two emitter resistors in the current mirror (e.g., R12 or R24). Then check the VAS bias current by measuring the voltage across the VAS emitter resistor R44 and dividing by the resistance of R44. Note how far off the VAS bias current is from the nominal 10 mA and in what direction. The approximate value of the necessary shunt resistance can be obtained from knowing that decreasing R27 by 10 Ω will cause a decrease in VAS current of about 1.8 mA. Conversely, decreasing R9 by 10 Ω will increase VAS bias current by about 1.9 mA. This approach should get the VAS current adequately close to the target value without iteration.

Selected LSK489 and LSJ689 JFET Pairs

If you purchase the boards for the DH-220C, you can optionally order them with SOT-23-6 LSK489 and LSJ689 JFETs that have been selected to yield VAS bias current within the recommended range when the IPS is biased to a total tail current of 4 mA. These devices will come soldered onto adapter boards that fit the holes in the board where a DIP-6 socket would go. For SOT-23 JFETs obtained independently, there are pads on the back side of the board for mounting them.

References

1. Bob Cordell, *LSK389 Application Note*, Linear Integrated Systems, January 2020, linearsystems.com.

2. Bob Cordell, *VinylTrak – A full-featured MM/MC phono preamp*, Linear Audio, vol. 4, September 2012, linearaudio.net.