The DH-220C MOSFET Power Amplifier

1. Introduction

Here we describe the circuit and adjustment of the DH-220C Lateral MOSFET Power Amplifier that was published as a construction project in the July and August 2021 issues of audioXpress magazine and co-authored with Rick Savas [1, 2, 3]. This document is an expanded version of the circuit description and testing portions of the original article.

The DH-220C amplifier is designed as an upgrade to the legendary Hafler DH-220 MOSFET power amplifier. The design is implemented on 2 PC boards, one as a drop-in replacement for the original circuit board and the other as a new board that consolidates all of the output stage wiring within the heat sink and under the main PCB. This design can also be used to upgrade the Hafler DH-200, P225 and P230 amplifiers (with the exception that the P230 employs 3 output pairs per channel and thus requires a different output board). The DH-500 and P500 can also be upgraded with appropriate PC boards.

The DH-220C uses most of the original infrastructure of the DH-220, including the chassis, power supply, heat sinks and original output stage lateral power MOSFETs (2SK134 and 2SJ49). The amplifier employs two output pairs and is capable of delivering over 120 W/8Ω using the original Hafler power supplies. Each output pair is biased at 200 mA for low crossover distortion.

The DH-220C incorporates a full-complementary JFET input stage and a push-pull VAS. The design also employs a DC servo for DC offset control.

2. The IPS/VAS

Figure 1 shows the IPS/VAS of the DH-220C. It is also referred to as the Analog Front End (AFE). The IPS/VAS is a full complementary JFET design using a floating tail. Although designed for use in a Lateral MOSFET amplifier, this IPS/VAS can be used with any type of output stage with the appropriate bias spreader. All bipolar transistors in the design are NPN 2N5551 or PNP 2N5401 unless noted.

Dual monolithic low-noise N-channel LSK489 and P-channel LSJ689 JFETs (from Linear Integrated Systems) are used for the input stage (IPS) [4]. Q9A and B, and Q10A and B form the floating full-complementary IPS, which operates at a tail current of 4 mA as determined by trimmer RV1 and R16. RV1 is required to trim the tail current to its design value because of the variability of JFET threshold voltages. Source degeneration resistors R9 and R27 decrease the transconductance of the P-channel long-tailed pair (LTP) to equal that of the N-channel LTP. The JFET LTPs are cascoded to allow for higher rail voltages than the JFETs would otherwise support.

Each LTP is loaded by a current mirror, which includes an emitter follower (EF) “helper” transistor to supply the base current for the mirror transistors. The V_{be} voltage drop of the helper transistor causes the differential collector voltages of the cascode transistors to be at the same DC potential. This is so because the subsequent two-transistor (2T) VAS also includes an emitter follower. This allows the use of the anti-parallel clamp diodes to limit differential voltage excursions to 1 diode drop. This

provides cleaner clipping and also helps prevent over-current in the VAS emitter follower transistor during clipping. 1N4149 clamp diodes are used because of their smaller capacitance as compared to the popular 1N4148.

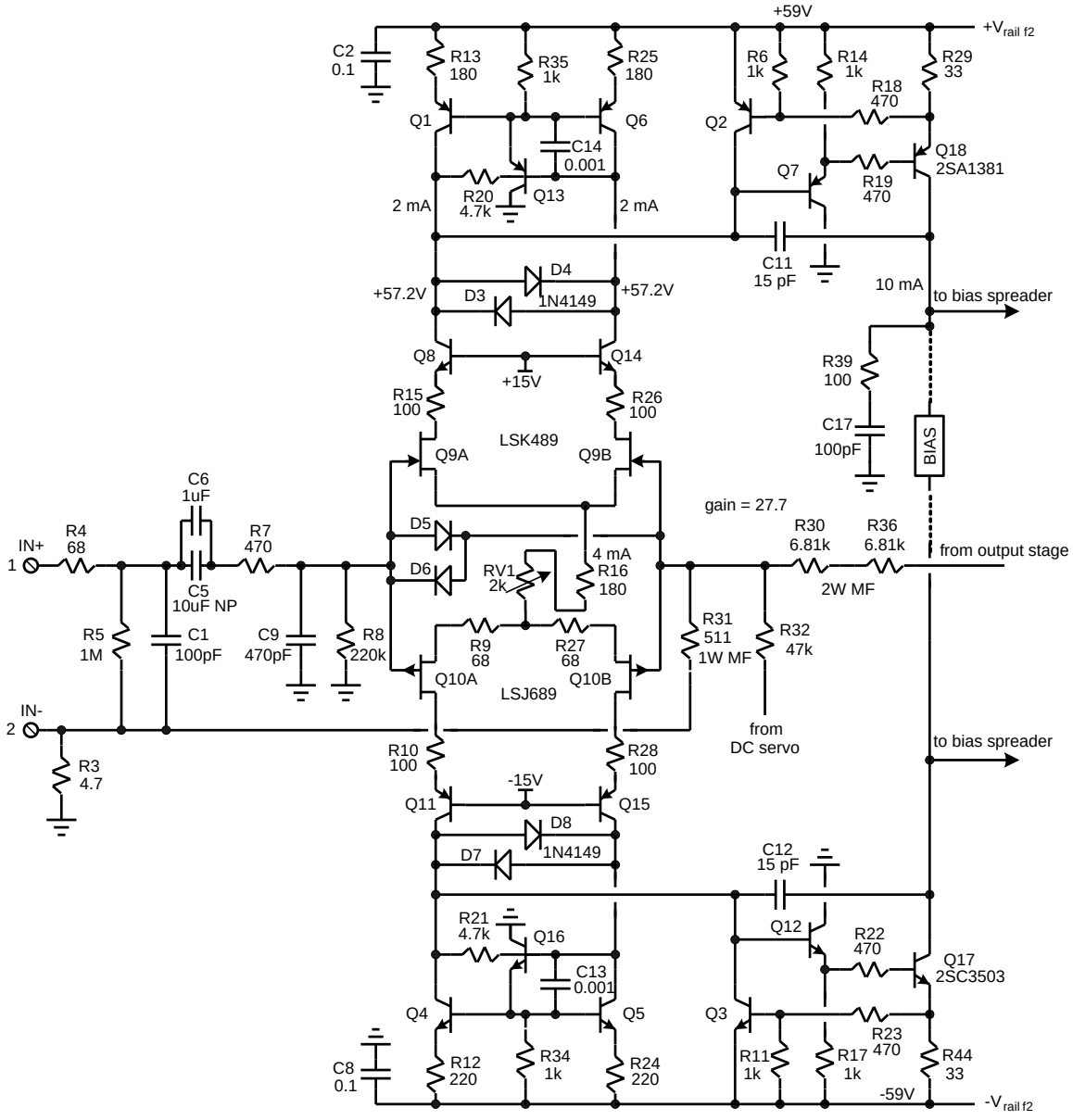

Figure 1: DH-220C IPS/VAS

Differential loading resistors R20 and R21 help stabilize the VAS bias current. Capacitors C13 and C14 reduce high-frequency interaction between the current mirror and the Miller-compensated 2T VAS by reducing the f_T of the helper transistors.

3. Input Network

The input network provides AC coupling and two sections of low-pass filtering (LPF) for good EMI immunity. The first LPF section employs R4 and C1. With a 50-Ω preamplifier source impedance, it will be down 3 dB at about 14 MHz. R4 and C1 also serve to form a Zobel network that terminates the interconnect cable at the amplifier in 68 Ω at high frequencies. The 68-Ω number is a compromise between the 50-Ω and 75-Ω characteristic impedances often found in coaxial interconnect cable. Terminating the interconnect in approximately its characteristic impedance causes the preamplifier to see a largely resistive load at high frequencies. This can improve stability and reduce EMI pickup at high frequencies. R7 and C9 form a second, more conventional input low-pass filter that is down 3 dB at about 600 kHz.

4. Feedback Network

The feedback network consisting of R31, R30 and R36 sets the closed-loop gain at 28 with fairly low feedback network impedance to reduce noise. 2 W metal film resistors R30 and R36 minimize feedback resistor distortion. The IPS/VAS is intended for use with a DC servo, and the offset correction signal is injected by R32. Offsets of ±140 mV can be corrected by the servo. The input coupling capacitor can often be eliminated because any DC offset from the external preamp is assumed to be smaller than this amount. This saves a quality input coupling capacitor that is usually redundant and may improve low frequency response.

5. Push-pull VAS

The push-pull VAS is a 2T design that includes Q7 and Q18 on the positive side and Q12 and Q17 on the negative side. VAS quiescent current is set to about 10 mA by the voltage drops across the current mirror emitter resistors R13/R25 and R12/R24. These voltage drops in turn depend on the 4 mA tail current in the IPS. Current-limiting transistors Q2 and Q3 are also present. R6 and R18 (and R11/23) provide some attenuation in the current-limiting feedback path in order to increase the current-limiting threshold by a factor of 1.5 to about 25 mA. In combination with the limited voltage swing from the IPS clamp diodes, VAS transistor base resistors R19 and R22 help limit the current in emitter followers Q7 and Q12 during clipping. They also limit stored charge in the bases of the VAS transistors Q18 and Q17 during clipping so as to allow the VAS transistors to come out of saturation more quickly. Operation of the emitter followers in the VAS (Q7 and Q12) at a healthy 1 mA also helps remove stored charge from the VAS transistors after a clipping event.

C11 and C12 provide Miller compensation to set the unity loop gain frequency (ULGF) at about 1.2 MHz. Zobel network R39/C17 stabilizes VAS output impedance at high frequencies and reduces peaking in the open-loop gain response.

6. DH-220C Bias Spreader and Drivers

Figure 2 shows the bias spreader and driver stage of the DH-220C. The bias spreader is a CFP design that typically supplies a spread of about 2.7 V to bias the output lateral MOSFETs and their BJT emitter follower drivers. The CFP bias spreader provides a stiff, low-impedance voltage drop that is advantageous for full complementary designs like this, wherein the VAS bias current can be somewhat more variable than in single-ended designs where the VAS bias current is set by a fixed current source. Trimmer RV2 is used to set the quiescent output stage bias to about 200 mA per output pair. 10-V Zener diodes D9 and D12 provide gate protection and current limiting for the

output MOSFETs by limiting their gate voltage with respect to the output rail to about ±10 V. R37 and R40 reverse-bias the Zener diodes by about 2.7 V under normal signal conditions to reduce their capacitance.

The output transistors are driven by emitter follower drivers that are biased at a healthy 16 mA so as to be able to drive the capacitances of the output MOSFETs with adequate turn-off current even under conditions of fast turn-off. The driver bias resistors provide a center-tap test point TP1 that allows measurement of output stage distortion alone or closure of the feedback loop without the output stage for testing purposes. This feature is implemented with header H1 and its jumper plug. Negative feedback is taken from either TP1 or the MOSFET sources in the output stage.

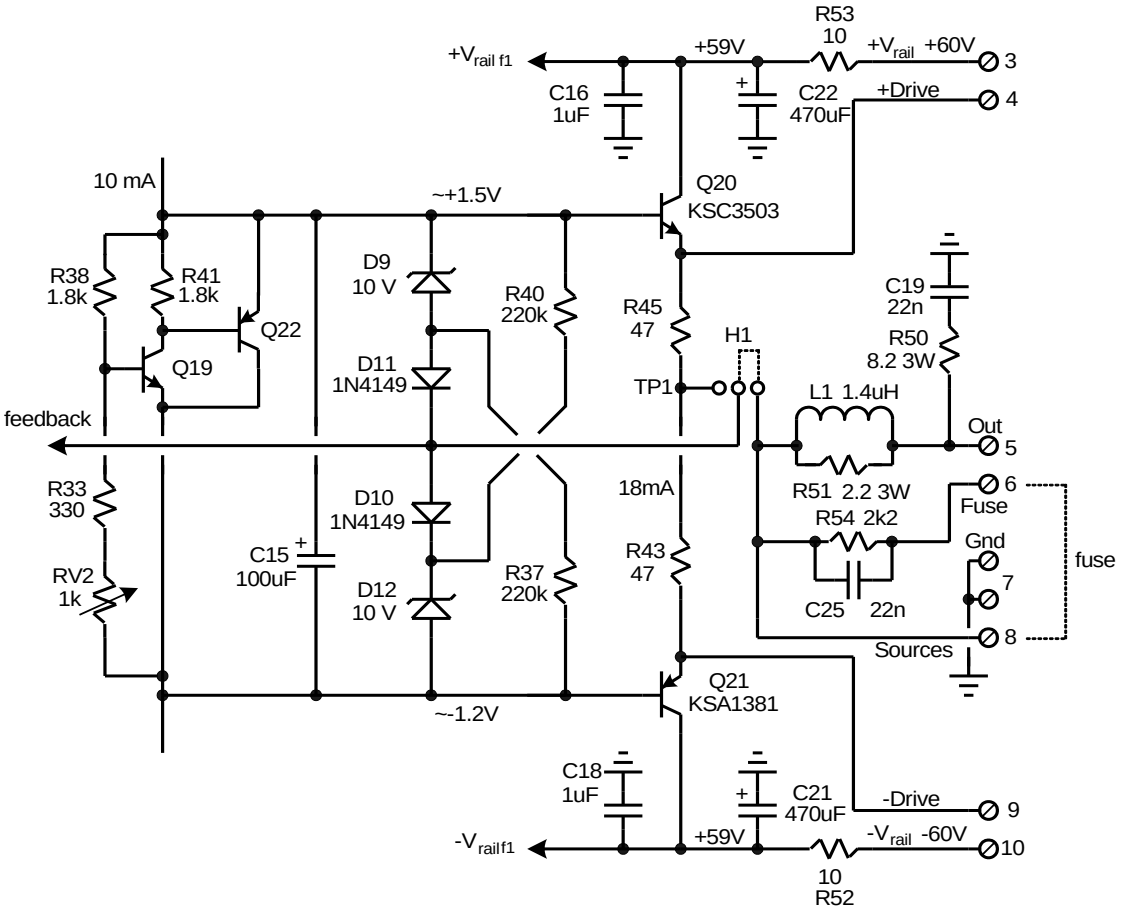

Figure 2: DH-220C bias spreader, drivers and output network

7. Output Stage

The output stage is implemented on a separate small PCB that lies underneath the main circuit board within the heat sink area. It replaces and consolidates all of the discrete fly-wiring that is used in the original design. It is shown in Figure 3. Gate stopper resistors are included with the same values as used in the original Hafler design. Two Zobel networks effectively in parallel (R4/C6 and R5/C4) allow the stabilizing action to be

physically close to each pair of MOSFET sources, minimizing inductance. This approach also avoids the need for a non-inductive wire-wound resistor, using instead two 3-W metal oxide film (MOF) resistors. The output board also includes generous bypassing in close proximity to the output transistors. These measures and the use of an output PCB with good high-frequency layout improve overall amplifier stability.

R8 is a 0.1-Ω resistor in series with the positive rail to the output MOSFETs. It allows monitoring of the output stage bias current for adjustment. Both ends of R8 are brought to PCB pads at the top of the board to allow measurement of its voltage drop. At output stage bias current of 400 mA, voltage drop across R8 will be 40 mV. At very high peak output current of 10 A, corresponding to about 200 watts into 4 ohms, voltage drop across this sensing resistor will only be 1 V. Diodes D3 and D4 protect the amplifier from rail voltage reversal in the event that one rail fails due to a blown fuse. Diodes D1 and D2 provide the usual protection against inductive loads causing the output node to snap outside the rail voltages. Quiescent current in each of the output transistors is set to about 200 mA. This healthy bias extends the “class-A” region and helps reduce crossover distortion. The class A region theoretically extends to about 2.5 watts into 8 ohms. Due to the transfer characteristics of lateral MOSFETs, the transition from the class A region into the class AB region is quite soft.

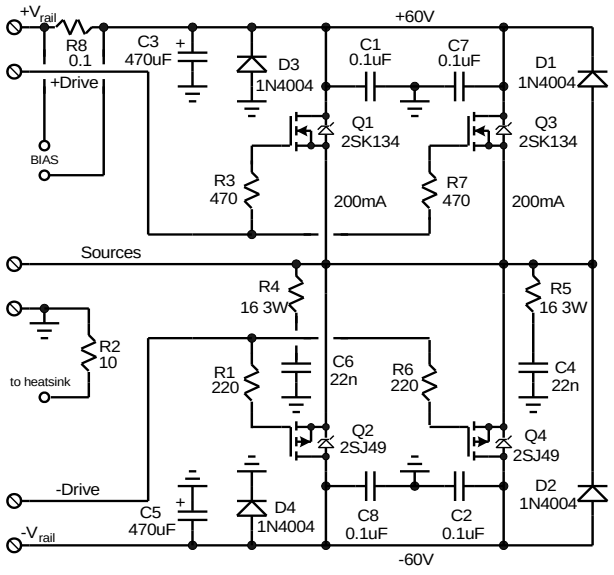

Figure 3: The DH-220C Output Stage

8. DC Servo

The DH-220C uses a DC servo as shown in Figure 4. The servo can correct up to 140 mV of input stage offset. DC servos function to control DC output offset in otherwise DC-coupled power amplifiers. A key advantage of DC servos is the elimination of the negative feedback electrolytic decoupling capacitor.

The concept of a DC servo is quite simple. The average DC level at the output is extracted by a low-pass filter, amplified and fed back to the feedback side of the input

stage. This drives the output DC value to zero or a very small value. This permits the use of a low-impedance DC-coupled feedback network while retaining high amplifier input impedance. In practice, an integrator is almost always used to provide both the low-pass filtering function and the gain. This is illustrated in Figure 4 where the input pair of the amplifier is implemented with JFETs. Without the DC servo, output offset would be 280 mV with a JFET offset of 10 mV.

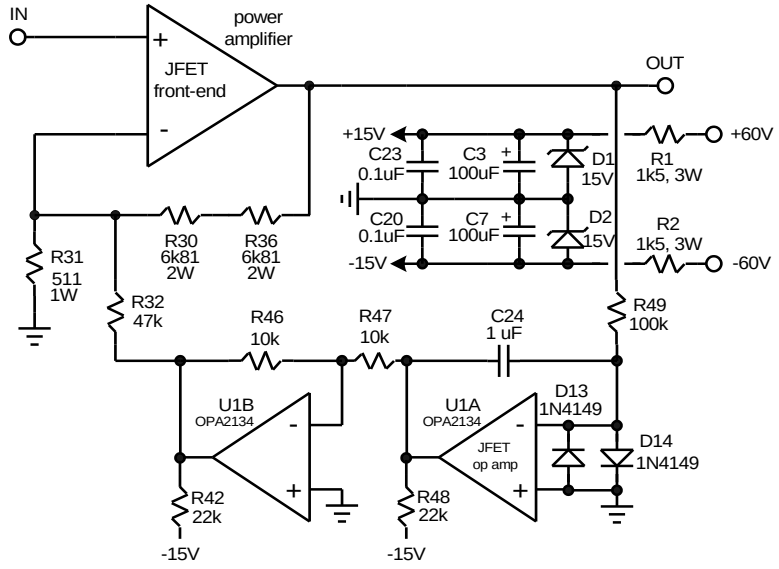

Figure 4: The DH-220C DC servo employs an inverting integrator.

The amplifier output is applied to a conventional inverting integrator U1A followed by a unity-gain inverter U1B to provide the proper feedback polarity. The integrator input resistor R49 is chosen to be 100 kΩ, while the integrator capacitor C24 is set to 1 μF. The integrator is usually implemented with a JFET op amp to avoid integrator offsets created by input bias current. U1 is an audio-quality OPA2134 JFET op amp. The integrator inputs are protected from excessive input voltages by diodes D13 and D14. The servo output from the inverter is applied to the feedback input of the amplifier input stage through a 47-kΩ resistor. If the op-amp output swings to 13 V, about 280 μA will flow into the feedback node, creating an effective correction voltage drop of about 140 mV across R31. The DC servo effectively creates an auxiliary feedback loop that is active at DC and very low frequencies.

If there exists a small positive average DC value at the amplifier output, integrator capacitor C24 will charge by the current sourced to it through R49, driving the output of the integrator negative. The output of the inverter will go positive and source current to the feedback input to drive the feedback input in a positive direction. This in turn will drive the output of the amplifier negative. The very high DC gain of the integrator forces the output of the amplifier to essentially zero. In practice, it forces the output voltage to equal the input offset voltage of the integrator op amp in the absence of input bias current. This will typically be less than ±10 mV for a JFET op amp.

On paper the complexity of the amplifier is higher with the use of a DC servo, but cost and space for the same quality is arguably lower than a high-capacitance non-polarized electrolytic in series with R31. The only major components are a dual op amp and a film integrating capacitor. The output of the servo drives the amplifier's feedback input node through a fairly high-value resistor (R32) because it needs only to inject enough correction current to overcome the maximum anticipated input-referred offset error. The large resistor tends to reduce the ability of the servo and its op amp to adversely impact sound quality via noise or distortion in the servo.

The servo provides increased negative feedback as frequency goes lower. As such it does indeed introduce a high-pass filter function into the audio path, but so does a simple electrolytic in the feedback return leg. With the DC servo, however, you have now removed an evil 100 µF (or more) electrolytic capacitor that would have been bad for the sound even if bypassed by a smaller film capacitor.

While some prefer JFET input pairs for reasons of sound quality and EMI resistance, there is another reason that makes them attractive. The JFET input stage does not suffer from DC offset caused by input bias current, and that makes the job of the DC servo much easier. If an amplifier is to have reasonably high input impedance, its input return resistor must be large (at least 20 kΩ). BJT input bias current flowing through this resistor can cause a far larger offset than the input voltage offset of the input pair or of input-referred offset from the VAS stage. If a JFET input stage is used instead, there is no DC offset from input bias current, and the servo need only compensate for the 5–15 mV of offset typical of a dual-matched monolithic JFET pair. Correcting ±10 mV of JFET input offset in the circuit of Figure 4 requires the servo op amp to produce only ±1 V. The bottom line here is that the servo must typically work much harder when used in a typical DC servo arrangement with BJT input pairs as opposed to JFET input pairs. The use of a JFET input stage permits the input of the DH-220C to be a high 220 kΩ. This places a very light load on the preamplifier and may improve the low-frequency response of its output coupling circuit.

The DC servo in Figure 4 is in the feedback path with modest gain at low frequencies. As such, the DC servo is in the signal path of the amplifier, and its performance can affect sound quality. The fact that it is injecting a signal at the input stage gives it opportunity to inject noise and distortion into the signal path. This can influence the quality of the audio signal, but is still better than having an electrolytic in the signal path. For this reason, audio-grade op amps are used for the DC servo’s integrator and inverter. Noise and class B crossover distortion created by the op amp can influence quality. In this design the outputs are pulled down by R42 and R48 to force the op-amp output stages to operate in class A.

The DH-220C has a closed loop gain equal to 28, set with the feedback resistors. The DC servo uses an inverting servo integrator with a 100-kΩ series resistor and a 1-µF capacitor. The integrator will have a gain of 1.6 at 1 Hz.

The 47-kΩ servo injection resistor R32 connects the servo inverter to the inverting input of the power amplifier, providing a servo attenuation factor of about 100:1. The servo loop gain at 1 Hz will be approximately the integrator gain times the ratio of R30 + R36 to R32. The latter equals 0.29. This means that the low-frequency cutoff created by the servo is at about 0.5 Hz (the servo-based LF cutoff is simply the

frequency where the servo loop gain falls to unity). Bear in mind that the overall amplifier low-frequency cut-off will also be influenced by the input coupling capacitor.

A system signal path often contains more coupling capacitors than necessary. There will usually be one at the output of the preamplifier, and yet another one at the input of the power amplifier. If the power amplifier has a DC servo, the input coupling capacitor of the amplifier can be bypassed, knowing that the DC output of the preamp is probably at or very close to zero. This is no more risky than using a DC-coupled power amplifier. Any small DC offset present at the input of the amplifier will be handled by the DC servo. In this case, an overall improvement in low-frequency transient response will have been had by the use of a DC servo. Removal of the input coupling capacitor is strictly a choice in regard to managing risk. Many DC-coupled power amplifiers have the option of switching in a blocking capacitor at the input.

9. DH-220C performance

The DH-220C clips at about 150 watts into 8 Ω and about 250 watts into 4 ohms. It is stable into a 2-Ω load and can deliver about 200 watts into a 2-Ω load with THD-1 less than 0.005% for short intervals. The core amplifier, without input and output low-pass filters, is down 3 dB at about 1.5 MHz. There is no peaking in the frequency response. The low-frequency 3-dB point lies below 2 Hz.

The A-weighted SNR is 104 dB referenced to 2.83 V at the output. Un-weighted SNR in a 20 kHz bandwidth is 100 dB. Input-referred noise is 6 nV/rt Hz. Slew rate is greater than 50 V/us. The 100 kHz square wave response into an 8-Ω load is nearly perfect, with 200 ns risetime. The amplifier has been verified to be stable with capacitive loads ranging from 1000 pF to 1 uF.

Damping factor of the DH-220C is over 500 up to 1 kHz. It falls to 70 at 20 kHz due to the impedance of the output coil.

Total Harmonic Distortion

Figure 5 shows measured 50-Hz THD+N versus power output with load resistances of 8 Ω, 4 Ω and 2Ω. Using the DH-220 power supply that delivered 56.5 V under load, the amplifier clipped at over 150 W and delivered over 120 W into 8 ohms with THD+N of 0.0008% at 50 Hz. There was no rise of distortion at low power levels. The dashed lines in the figure indicate readings that were noise as opposed to distortion.

Just below clipping, the DH-220C delivered 240 watts at 50 Hz into 4 ohms with about 0.0015% THD+N. At 200 watts, THD+N was about 0.0006%. It was able to deliver over 150 watts into a 2-Ω load with THD+N less than 0.0012%.

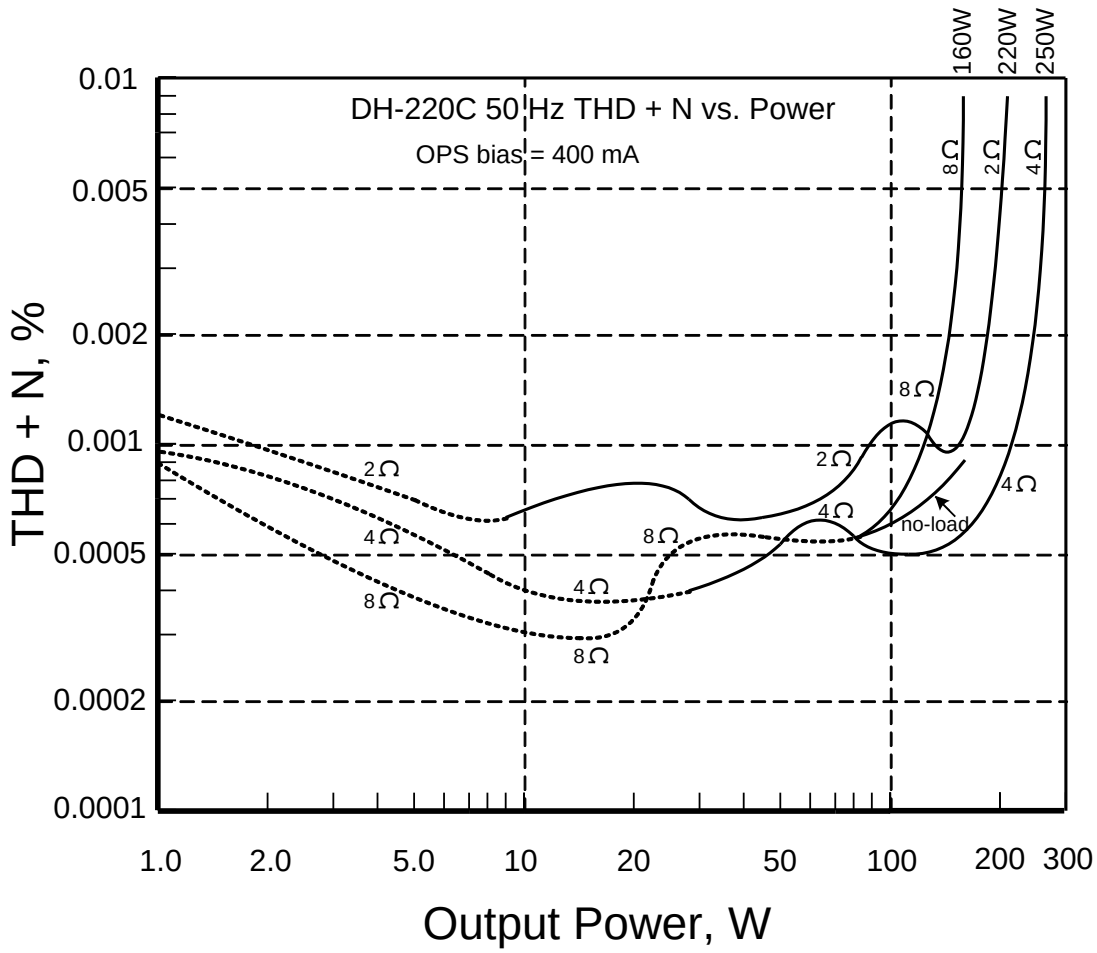

Figure 5: THD + N vs. Power at 50 Hz

Figure 6 shows measured 1-kHz THD+N versus power output into 8 Ω, 4 Ω, 2 Ω and no-load. With the DH-220 power supply delivering 56.5 V under load, the amplifier clipped at over 150 W with an 8-Ω load. It delivered over 120 W into 8 ohms with THD+N of 0.0015% at 1 kHz. There was no rise of distortion at low power levels. THD-1 was below 0.0011% in the critical power range between 1 W and 10 W. The dashed lines in the figure indicate readings that were noise as opposed to distortion.

The DH-220C clipped at 240 watts into a 4-Ω load and delivered 200 watts with THD-1 of less than 0.003%. The amplifier was able to deliver 200 watts for short intervals into a 2-Ω load with THD-1 of about 0.005%. After about 5 seconds, heating of the lateral MOSFETs increased their *on* resistance and reduced the power delivered at clipping.

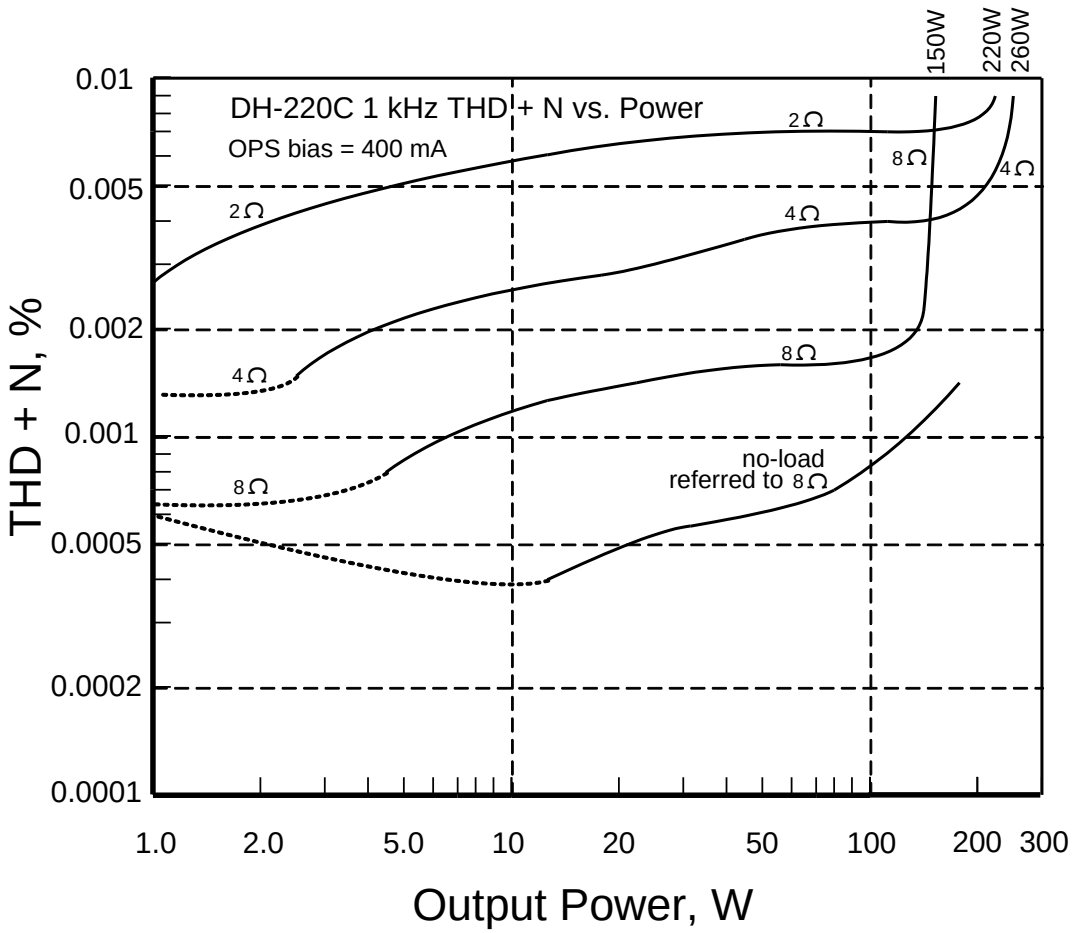

Figure 6: THD + N vs. Power at 1 kHz

Figure 7 shows measured 20-kHz THD+N versus power output into 8 Ω, 4 Ω, 2 Ω and no-load. The DH-220C delivered over 120 W into 8 ohms with THD+N of 0.018% at 20 kHz. There was no rise of distortion at low power levels. THD-20 was below 0.014% in the critical power range between 1 W and 10 W. The dashed lines in the figure indicate readings that were noise as opposed to distortion.

The DH-220C delivered 200 watts into a 4-Ω load with 20-kHz THD+N of 0.06%. With a 2-Ω load, the amplifier was able to deliver almost 200 watts into a 2-Ω load with THD+N of 0.12%.

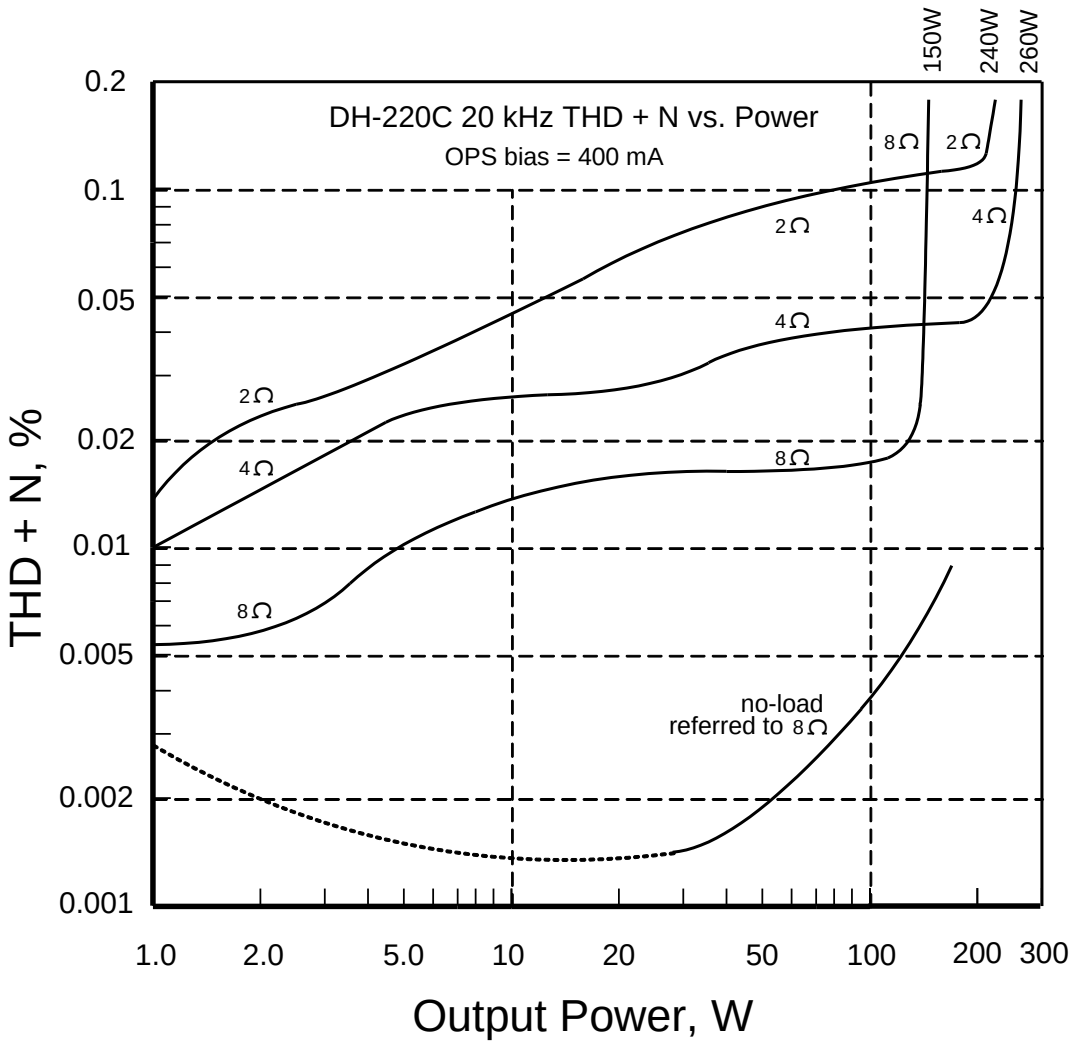

Figure 7: THD + N vs. Power at 20 kHz

Figure 8 shows measured 20-kHz THD+N versus power output for the output stage alone into 8 Ω, 4 Ω and 2 Ω. This shows that output stage distortion dominates, and comparison with Figure 7 allows one to see the reduction due to negative feedback around the output stage. THD+N is about 0.3% into 8 Ω at 100 W, about 0.5% into 4 Ω at 200 W, and 0.8% into 2 Ω at 180 W. Measurements were made by closing the global negative feedback loop from the drivers. This leaves the output stage with no negative feedback to reduce distortion.

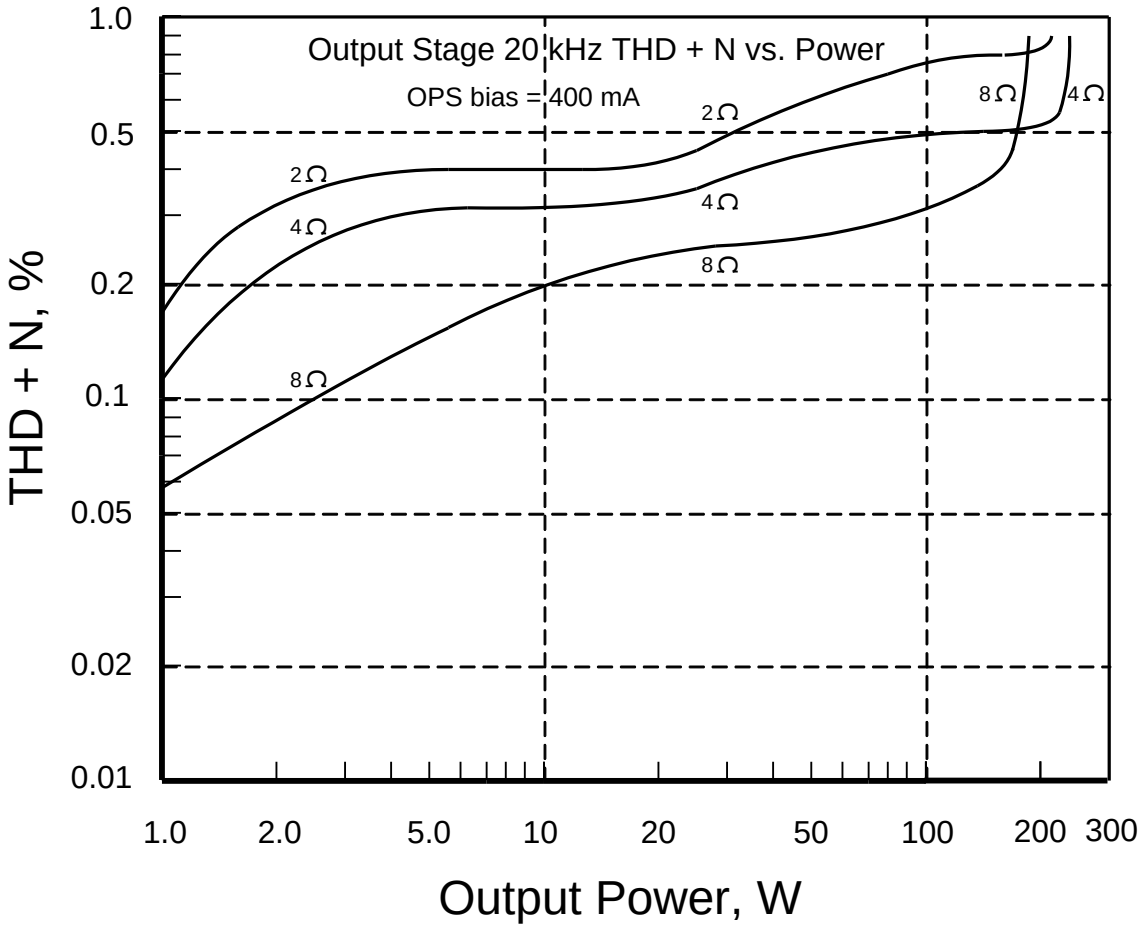

Figure 8: THD-20 for MOSFET Output Stage Alone

10. Adjustments

There are three adjustments needed for the DH-220C. The first is adjustment of IPS bias current by trimmer VR1. The second is adjustment of the output stage bias current by trimmer VR2. The third adjustment, which may not be needed, is to adjust the VAS bias current. This is needed if the input offset voltages of the N-channel and P-channel IPS JFETs are significantly different. If necessary, this adjustment is carried out by adding a shunt trim resistor in parallel with one of the source degeneration resistors associated with the P-channel pair.

When making adjustments to the trim pots, It is recommended that you employ a small screwdriver with most of its shaft insulated by heat-shrink tubing. Similarly, when probing the circuit board, you may wish to use a meter probe with most of its metal probe shaft insulated by heat-shrink tubing. These measures will help prevent accidental short circuits caused by non-insulated portions of these tools.

Input Stage Bias Current

The adjustment procedure is begun by turning both trimmers to their full CCW position, corresponding to minimum IPS and OPS bias current, before turn-on.

Trimmer VR1 is advanced clockwise until IPS bias current is 4.0 mA. For this measurement, the IPS bias current can be monitored as the current through R16 to be 4.0 mA, or the current through R12 or R24 to be 2.0 mA. Resistor R16 is 180 ohms, so the voltage across R16 should be set to 720 mV. Resistors R12 and R24 are each 220 ohms, so the voltage across R12 or R24 should be set to 440 mV. IPS bias current is not critical, and can generally be allowed to be between 3.5 mA and 4.5 mA.

Note that in this design it is not necessary to match I_{DSS} between the N-channel and P-channel devices. This is because the transconductance of a JFET from the same process is only a very mild function of I_{DSS} or threshold voltage.

VAS Bias Current

The target value for VAS bias current is 10 mA, but it is also not critical and can lie between 8 mA and 12 mA. Changes in IPS bias current affect VAS bias current in a proportional way. Additionally, input offset voltages of the N-channel and P-channel input pairs affect VAS bias current for a given IPS bias current. VAS bias current is monitored by measuring the voltage across R44, the 33-Ω emitter degeneration resistor for VAS transistor Q17. If VAS current is 10 mA, the voltage across R44 will be 330 mV.

If the N- and P-channel pairs have the same amount of offset voltage in the same direction, there will be virtually no influence on VAS bias current; there will just be some influence on overall input stage offset, which will be corrected by the DC servo. However, if the two pairs have different offsets in the same direction, there will be some influence on VAS bias current that may be large enough to need some correction for VAS bias current to be between 8 mA and 12 mA. If the two pairs have offsets that are in opposite directions, there will be a more significant influence on VAS bias current, and the need for correction will be more likely.

If socketed JFETs are being used, one of them can often be reversed, so that its offset direction is reversed. This can often reduce VAS bias current deviation from the target range adequately.

If soldered SMT JFETs are being used, the effective offset of the P-channel devices can be altered by shunting one of the 68-Ω source resistors (R9 and R27) by a larger tweaking resistor that may reduce the value of the shunted resistor by perhaps 10% to 20%. The nominal voltage drop across these 68-Ω resistors with 2 mA flowing through them is about 135 mV, so it is easy to see that reducing one of them by only 10% can change the effective offset of the P-channel pair by about 13.5 mV. In this example a 750-Ω shunt would be used, and it changes the VAS bias current by about 1.0 mA. The idea is not to make the effective offset of the P-channel pair to be zero, but rather to make that offset closer to being the same amount as that of the N-channel pair and in the same direction. Creating a small difference between the values of R9 and R27 will have a negligible effect on amplifier performance.

If the VAS bias current is too low, R9 should be shunted to reduce its value. If the VAS current is too high, R27 should be shunted to reduce its value. The shunting resistors can be soldered directly in parallel with the chosen resistor on the component side of the board. Knowing amount and direction of the VAS bias current deviation from the target allows one to estimate the value of the needed shunt resistor and onto which of R9 and R27 it should be connected in

parallel. Decreasing the value of a source resistor by 10 Ω (about 15%, corresponding to a parallel resistance of about 390 Ω) will change VAS bias current by about 2.1 mA.

Output Stage Bias Current

Output stage bias current is adjusted by advancing RV2 in a clockwise direction until the total output stage bias current is between 350 mA and 400 mA. OPS bias current is monitored by measuring the voltage drop across R8 on the OPS board. R8 is 0.1 ohms, so the target voltage across R8 should be between 35 mV and 40 mV. OPS bias current should be re-adjusted after the heat sink has warmed up.

11. Summary

The DH-220C provides an upgrade path for the original Hafler DH-220 that includes a full-complementary JFET input stage and a DC servo, among other circuit improvements. Reduced EMI susceptibility has also been implemented in the design. A separate output board consolidates and replaces the discrete wiring employed in the original Hafler design and places decoupling capacitors and the output Zobel network closer to the output transistors, improving stability and reducing radiated nonlinear magnetic fields that can introduce distortion into the input stage.

More information can be found in the July and August 2021 issues of auioXpress, including pictures and a build guide. Printed wiring boards are available from Rick Savas via eBay. Boards can optionally be purchased with suitable 2SK489 and 2SJ689 JFETs included.

12. References

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